





UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,872	05/31/2001	Richard P. Mackey	10559-389001	.1080
20985 75	590 01/30/2004		EXAMINER	
FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			PUENTE, EMERSON C	
		·	ART UNIT	PAPER NUMBER
•			2113	_5
		DATE MAILED: 01/30/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

,	eply		09/872,872 Examiner		MACKEY ET AL.						
,	he MAILING DATE of this commu										
- T	eply			į	Art Unit						
T	eply		Emerson C	Puente	2113						
	• •	пісацоп арре	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHOR THE MAI - Extension after SIX ( - If the peri - If NO peri - Faiture to - Any reply	ILING DATE OF THIS COMMUN is of time may be available under the provision (6) MONTHS from the mailing date of this commod for reply specified above is less than thirty od for reply is specified above, the maximum reply within the set or extended period for repreceived by the Office later than three months tent term adjustment. See 37 CFR 1.704(b).	NICATION.  ns of 37 CFR 1.136  nmunication.  (30) days, a reply obtained will  by will, by statute, of	6(a). In no event within the statuto ill apply and will e cause the applica	ory minimum of thirty (30) days expire SIX (6) MONTHS from to ation to become ABANDONED	ely filed will be considered timely. he mailing date of this communication. (35 U.S.C. § 133).						
1)⊠ Re	Responsive to communication(s) filed on 31 May 2001.										
2a) ☐ Th	is action is FINAL.	2b)⊠ This a	action is non	ı-final.							
	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.										
Disposition of Claims											
4a) 5)□ Cla 6)⊠ Cla 7)□ Cla	Claim(s) is/are pending in the application.  4a) Of the above claim(s) is/are withdrawn from consideration.  Claim(s) is/are allowed.  Claim(s) 1-16 is/are rejected.  Claim(s) is/are objected to.  Claim(s) are subject to restriction and/or election requirement.										
Application	•		0.000.00	•							
	e specification is objected to by t	he Examiner	r.								
,	e drawing(s) filed on is/are			] objected to by the E	xaminer.						
Ap	plicant may not request that any obj	ection to the d	drawing(s) be	held in abeyance. See	37 CFR 1.85(a).						
	placement drawing sheet(s) including										
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.											
-	Priority under 35 U.S.C. §§ 119 and 120										
12)											
Attachment(s)											
2) Notice of	References Cited (PTO-892) Draftsperson's Patent Drawing Review ( on Disclosure Statement(s) (PTO-1449)		5	· <u> </u>	PTO-413) Paper No(s) stent Application (PTO-152)						

} .

Art Unit: 2113

## **DETAILED ACTION**

This action is made Non-Final. Claims 1-16 have been examined.

## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 15 and 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regards to claim 15, "generating two output signals to the memory controller based on the delay signal" is inconsistent with the specification. In the specification, applicant discloses transmitting a reset signal and a power delay signal to the memory controller based on reset condition (see page 3 bottom full paragraph).

In regards to claim 16, the phrase "preventing initiating the data retention routine if the reset signal is not de-asserting for a predetermined period of time" is contradictory to the specification. In the specification, applicant disclose "if the reset signal is detected long enough and either a power failure or an external reset event is detected, the memory controller self refresh state machine will execute. Once the self refresh sequence has been performed, the memory controller would enter the reset state" (see page 4 top paragraph) indicating initiating the data retention routine if the reset signal is not de-asserting for a predetermined period of time,

Art Unit: 2113

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,182,687 of Campbell et al. referred hereinafter "Campbell".

In regards to claim 1, Campbell discloses:

detecting a reset condition (see column 17 lines 35-42);

verifying a memory controller is initialized (see column 17 lines 42 to column 18 lines 15); and

placing a memory system into a retention state (see column 18 lines 9-15 and 35-50).

In regards to claim 2, Campbell discloses verifying the memory controller is initialized by delaying a reset signal (see column 18 lines 9-15).

In regards to claim 3, Campbell discloses monitoring the voltage level of a system to determine a power (see column 17 lines 35-42).

In regards to claim 4, Campbell discloses generating a reset condition when either a power failure or a reset request occurs (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 5, Campbell discloses verifying the reset request does not occur prior to initialization (see column 18 lines 9-15).

In regards to claim 6, Campbell discloses detecting the reset condition and verifying the memory controller is initialized external to the memory controller (see column 18 lines 9-15).

Art Unit: 2113

In regards to claim 7, Campbell discloses

a power delay circuit external to a memory controller, wherein the power delay circuit instructs the memory system to run a retention routine during a power failure or reset condition. Campbell discloses a power monitor circuit (see figure 9a item 230) that instructs a reset after power failure or reset condition (see column 17 lines 53-55).

In regards to claim 8, Campbell discloses a power fail controller, which prevents the retention routine from executing when the memory system is not configured. Campbell discloses a reset circuit that provides a delay reset signal enabling a power down routine before resetting (see figure 9a item 242 and column 18 lines 9-15).

In regards to claim 9, Campbell discloses wherein the power delay circuit outputs a reset signal if either a power failure or a system reset signal is detected (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 10, Campbell discloses wherein the power delay circuit outputs a delay signal when the output reset signal is caused by a system reset signal. Campbell discloses a reset circuit that provides a delayed reset signal, indicating a delay signal when the output reset signal is caused by a system reset signal (see column 17 lines 53 to column 18 lines 15).

In regards to claim 11, Campbell discloses wherein the power delay circuit monitors a voltage detector to detect a power failure (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 12, Campbell discloses the power fail controller may be internal to the memory controller (see figure 9a item 242).

In regards to claim 13, Campbell discloses

detecting either a power failure or reset signal (see column 17 lines 38-42);

Art Unit: 2113

generating a delay signal based on the reset signal (see column 18 lines 9-15); and initiating a data retention routine if the delay signal indicates the memory system is initialized. Campbell discloses resetting after a power down routine, indicating initiating a data retention routine if the delay signal indicates the memory system is initialized (see column 18 lines 9-15 and 35-50).

In regards to claim 14, Campbell discloses monitoring the voltage level of a system to determine a power failure (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 15, Campbell discloses generating two output signals to the memory controller based on the delay signal (see figure 9a item 270 and 234 and column 17 lines 40-50 and column 18 lines 5-15).

In regards to claim 16, Campbell discloses preventing initiating the data retention routine if the reset signal is not de-asserted for a predetermined period of time (see column 17 lines 53 to column 18 line 15).

## Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (703) 305-8012. The examiner can normally be reached on 8-5 M-F.

Art Unit: 2113

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5631.

Emerson Puente 1/23/04

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER

TECHNOLOGY CENTER 2100